Abstract of the Disclosure

An amplitude limiting circuit for limiting the amplitude of a signal input to a power amplifier includes an amplitude converter, determination unit, peak detector, window filter, delay circuit, and multiplier. The amplitude converter calculates the amplitude value of an input signal. The determination unit detects, as a detection interval, an interval in which the amplitude value exceeds a threshold, on the basis of a preset threshold and the amplitude value of the input signal. The peak detector detects, in the detection interval, the peak time when the maximum amplitude value appears and an amplitude value at the peak time as a peak value. The window filter generates a window function for limiting the amplitude value to a value not more than the threshold by using the peak value output from the peak detector. The delay circuit delays the input signal such that the peak time output from the peak detector coincides with the time when the window function output from the window filter exhibits the minimum value. The multiplier multiplies an output signal from the delay circuit by the window function. An CDMA communication apparatus is also disclosed.